new claims 61-70 for consideration by the Examiner. Applicants believe that no new matters have been introduced.

Claims 39-40, 44, and 60 are rejected under 35 U.S.C. § 112, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claims 39-40, 44, and 60 have been amended to more clearly recite aspects of the invention. Withdrawal of the rejection is respectfully requested.

Claims 30-44 and 59-60 stand rejected under 35 U.S.C. § 102(e) as anticipated by, or, in the alternative, under 35 U.S.C. § 103(a) as obvious over *Watts et al.* (5,985,748). The Examiner asserts that *Watts et al.* discloses a two-step process for planarizing a copper layer with the first step removing copper material at a rate of 3,800 A/min and the second step removing copper at a rate of 1,600 A/min, and that it would have been obvious to employ any of a variety of different CMP polishing process parameters in the process taught in *Watts et al.* Applicants respectfully traverse this rejection.

Watts et al. discloses a combination of polishing steps including a first step using a first slurry containing an abrasive component and a chemical component, and a second polishing step using a second slurry having a reduced amount of the abrasive component. *Watts et al.* does not teach, show, or suggest polishing the substrate surface with a first abrasive-free polishing composition to reduce a copper or copper alloy layer at a first removal rate and polishing the substrate with a second abrasive-free polishing composition to remove the copper or copper alloy layer at a second removal rate less than the first removal rate. Therefore, *Watts et al.* does not teach, show, or suggest claimed aspects of the invention.

The Examiner also has taken official notice to the following: that a separate CMP polishing step to polish a diffusion barrier is conventional or at least well known in the CMP polishing arts; that recycling a CMP slurry is conventional or at least well known in the CMP polishing arts; that using rinse steps after a CMP polishing step to remove the CMP slurry is conventional or at least well known in the CMP polishing arts; and that usage of an anticorrosive rinse step on a CMP polished wafer is conventional or at least well known in the CMP polishing arts.

Applicants traverse the Examiner's Official Notice that a separate CMP polishing step to polish a diffusion barrier is conventional or at least well known in the CMP polishing arts and request that the Examiner provide support for such a position as detailed under MPEP 2144.02.

Applicants traverse the Examiner's Official Notice that recycling a CMP slurry is conventional or at least well known in the CMP polishing arts since conventional CMP polishing processes discard CMP compositions, such as abrasive containing compositions, rather than recycling such compositions due to the presence of contaminants in the post-polishing CMP compositions. Applicants request that the Examiner provide support for such a position as detailed under MPEP 2144.02.

Applicants traverse the Examiner's Official Notice that using rinse steps after a CMP polishing step to remove the CMP slurry is conventional or at least well known in the CMP polishing arts and request that the Examiner provide support for such a position as detailed under MPEP 2144.02.

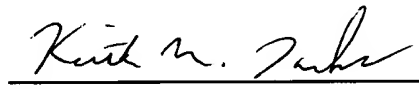
Applicants traverse the Examiner's Official Notice that usage of an anticorrosive rinse step on a CMP polished wafer is conventional or at least well known in the CMP polishing arts on grounds that there is no suggestion or motivation in *Watts et al.* nor the Examiner's Official Notice to expose a polishing pad disposed on the first platen or the substrate surface to an inhibitor after polishing at the first removal rate and prior to polishing at the second removal rate as recited in claim 42; and that there is no suggestion or motivation in *Watts et al.* nor the Examiner's Official Notice to that there is no suggestion or motivation in *Watts et al.* nor the Examiner's Official Notice to expose a polishing pad disposed on the second platen or the substrate surface to an inhibitor after polishing at the second removal rate and prior to removing the barrier layer as recited in claim 43. Applicants request that the Examiner provide support for such a position as detailed under MPEP 2144.02. Applicants respectfully request withdrawal of the rejection.

The prior art made of record is noted. However, it is believed that the secondary references are no more pertinent to the Applicants' disclosure than the primary references cited in the office action. Therefore, it is believed that a detailed discussion

of the secondary references is not deemed necessary for a full and complete response to this office action. Accordingly, allowance of the claims is respectfully requested.

In conclusion, the references cited by the Examiner, neither alone nor in combination, teach, show, or suggest the claimed aspects of the invention. Having addressed all issues set out in the office action, applicants respectfully submit that the claims are in condition for allowance and respectfully request that the claims be allowed.

Respectfully submitted,



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App ndix

Please replace the paragraph at page 11, line 14, to page 12, line 8, with the following paragraph:

Embodiments of the present invention include a multi-step process comprising: (a) CMP on a first rotating or linear platen employing a fixed abrasive polishing pad or a conventional, non-fixed abrasive polishing pad using an abrasive or abrasive-free chemical agent, at a high removal rate to remove most of the bulk Cu overburden; and (b) CMP on a second rotating or linear platen employing a fixed abrasive polishing pad or a conventional, non-fixed abrasive polishing pad using an abrasive or abrasive-free chemical agent, at a reduced removal rate with high selectivity to and stopping on the Ta or TaN barrier layer. Buffing on a third rotating or linear polishing pad can then be conducted, using an abrasive slurry, to remove the Ta or TaN barrier layer. A suitable buffing technique is disclosed in co-pending U.S. patent application Serial No. [_____ filed on _____ (Attorney Docket No. 49959-063; Client Reference No. 003929)] 09/401,643, filed on September 22, 1999, the entire disclosure of which is incorporated by reference herein. The surface of the silicon oxide interlayer dielectric is also buffed to reduce or eliminate scratching and defects. The polishing pads are mounted on rotating platens. Multi-station CMP systems are commercially available, such as the Mirra® polisher, available from Applied Materials, Inc., Santa Clara, California.

Please replace the paragraph at page 14, line 15, to page 15, line 2, with the following paragraph:

For example, in an interconnection system comprising a silicon dioxide interlayer dielectric and TaN barrier layer, the chemical agent can comprise about 1 to about 10 wt.% of an oxidizer, e.g., about 6 wt.%, such as hydrogen peroxide, about 0.05 to about 0.20 wt.% of an inhibitor, e.g., about [1.5] 0.15 wt.%, such as 5-methyl benzotriazole, about 1.0 to about 5.0 wt.% e.g., about 3 wt.%, of a chelating agent, such as iminodiaetic acid, and about 3.0 to about 15.0 wt.%, e.g., about 9.0 wt.%, of another chelating agent,

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such as ammonium hydrogen phosphate, the balance deionized water. The pressure is typically about 3 psi. The concentration of the inhibitor can be strategically adjusted throughout the polishing steps of the present invention to control the static etching rate. For example, the static etching rate can be decreased by increasing the amount of inhibitor, thereby reducing chemical complexing of Cu by chelating components of the chemical agent.

Please replace the paragraph at page 16, lines 7-29, with the following paragraph:

The wafer surface is then buffed, in a conventional manner or as disclosed in a pending U.S. patent application Serial No. [_____, filed in _____ (Attorney Docket No. 49959-062; Client Reference No. 003929)] 09/401,643, filed on September 22, 1999, with abrasive, to remove the Ta or TaN barrier layer, under conditions such that there is no or reversed selectivity among the silicon oxide interlayer dielectric, barrier layer and Cu. Embodiments of the present invention comprise further refinements to minimize dishing. It was found that dishing can be controlled during CMP steps (a) and (b) by controlling one or more processing features or parameters. For example, embodiments of the present invention comprise controlling the polishing pad surface at a temperature at no greater than about 44°C, as by reducing the platen rotating speed to no greater than 40 rpm, thereby reducing static etching and, hence, dishing. It should be appreciated that the static etching rate should not be reduced to the extent that the polishing by-products generated during CMP can not be removed, e.g., dissolved. The polishing by-products generated during CMP can be flushed away with a high flow of chemical agent which can be recycled to reduce the cost of consumables.

IN THE CLAIMS:

Please cancel claims 45-58 without prejudice, and amend the following claims:

30. (Amended) A method of planarizing a substrate surface containing a copper or copper alloy layer disposed on a barrier layer comprising:

(a) polishing the substrate surface on a first platen with a first abrasive-free polishing composition to reduce a copper or copper alloy layer at a first removal rate; and

(b) polishing the substrate on a second platen with a second abrasive-free polishing composition to remove the copper or copper alloy layer at a second removal rate less than the first removal rate.

32. (Amended) The method according to claim 30, wherein the first removal rate is greater than about 5,000 Å per minute and the second removal rate is between about 1000 Å per minute and about 3,000 Å per minute.

34. (Amended) The method according to claim 30, wherein polishing at the second removal rate is performed at a [selectivity] removal rate ratio of copper [:] layer to barrier layer of greater than about 100:1.

36. (Amended) The method according to claim 35, wherein [polishing at the first and second removal rates are performed on a] the first platen and the second platen each comprise a polishing pad mounted on a rotating, stationary, or linear platen [fixed abrasive polishing pad mounted on the first and second platens].

37. (Amended) The method according to claim 36, wherein the first and second platens are rotated during polishing [at the first and second removal rates] at less than about 60 rpm or first and second belts disposed on the first and second platens are moved linearly at a rate of less than about 30 inches per second.

38. (Amended) The method according to claim 36, further comprising cleaning the polishing pads by removing debris and polishing by-products [between each substrate].

39. (Amended) The method according to claim [36] 30, further comprising recycling the [chemical agent] first abrasive-free polishing composition, the second abrasive-free polishing composition, or both.

40. (Amended) The method according to claim 36, wherein [the chemical agent is] the first abrasive-free polishing composition is delivered to the [polishing pad or the substrate surface] first platen at a flow rate of about 300 milliliters per minute or [more] greater and the second abrasive-free polishing composition is delivered to the second platen at a flow rate of about 300 milliliters per minute or greater.

41. (Amended) The method according to claim 36, wherein the static removal rate of the [substrate surface] copper or copper alloy by the first abrasive-free polishing composition and the second abrasive-free polishing composition is about 150 Å per minute or less.

42. (Amended) The method according to claim [36] 30, further comprising exposing [the] a polishing pad disposed on the first platen or the substrate surface to an inhibitor after polishing at the first removal rate and prior to [initiating] polishing at the second removal rate.

43. (Amended) The method according to claim [31] 42, further comprising exposing [the] a polishing pad disposed on the second platen or the substrate surface to an inhibitor after polishing at the second removal rate and prior to [initiating] removing the barrier layer.

44. (Amended) The method according to claim [30] 36, further comprising:

exposing the first polishing pad or the substrate surface to an inhibitor after polishing at the first removal rate and prior to polishing at the second removal rate;

exposing the second polishing pad or the substrate surface to an inhibitor after polishing at the second removal rate; and

[recirculating the chemical agent] recycling the first abrasive-free polishing composition, the second abrasive-free polishing composition, or both.

59. (Amended) A method of planarizing a wafer surface, comprising:

a step for removing a portion of a copper containing material with a first abrasive-free polishing composition at a first removal rate; and

a step for selectively removing a copper containing material with a second abrasive-free polishing composition at a second removal rate less than the first removal rate.

60. (Amended) The method of claim 30, wherein [chemical mechanical polishing (CMP) the wafer to reduce the copper or copper alloy layer at a first removal rate to a thickness of about 500Å to about 3,000 Å and CMP the wafer to remove the copper or copper alloy layer at a second removal rate, less than the first removal rate, stopping on the barrier layer] the method steps for processing a substrate surface comprise a series of instructions disposed in comprise a computer-readable medium [bearing] adapted to implement instructions for planarizing the wafer surface by a chemical mechanical (CMP) system when said instructions are arranged and executed by one or more processors connected to the chemical mechanical (CMP) system.